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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/672,790	09/26/2003	John Banning	TRAN-P243	9488

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EXAMINER	
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ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/672,790	BANNING ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07/16/07,03/20/07*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) *8-45* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. Claims 1-7 are presented for examination.

2. Claims 8-45 withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected inventions, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on 07/16/07.

3. Applicant's election with traverse of Group I in the reply filed on 07/16/09 is acknowledged. The traversal is on the ground(s) that :

a) all recited claims were previously examined. All claims were rejected by a single rejection. Therefore, previous examination appears to infer the examination is not seriously burdensome;

b) claim 1 is not directed to software development or software development tools or testing or debugging or analysis of program execution as set forth in class 717, subclass 131;

c) claim 17 is not data driven or demand driven processor;

d) claim 23 is not directed to analysis of code form , parsing or syntax analysis

This is not found persuasive because :

4. As to a) above, previous examination does not necessarily mean that examination was not seriously burdensome. Nowhere does MPEP state that a single rejection must not be restricted. Restriction is applicable to claims, not prior art. In fact, the examination was seriously burdensome and examiner will show how below in this action.

5. As to b), claim 1 clearly recites a trigger pattern in a first machine language and modifying the instruction segment to form a second machine language without the feature of the accessing instruction modification information from a memory responsive to the trigger pattern in the first machine language. Therefore , it is directed to a method of software program development under 717/131 while, for example, the Group II

presents another functional part of which is directed to a memory for accessing the instruction modification information under class 712/248. Therefore, Group I and group II are subcombinations usable together (see also Pages 3,4 set forth in the restriction requirement on 06/12/07).

6. As to c), claim 17 is recited as having a processor coupled to a memory for executing machine language and implementing the method. Therefore, it is a data driven. The evidence is the processor is being coupled to a memory, not processor alone. Inventions I (claim 1) and III (claim 17) are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct if they do not overlap in scope and are not obvious variants, and if it is shown that at least one subcombination is separately usable, in the instant case, subcombination I has separate utility such as a system ***which does not have the processor coupled to the memory for executing machine language instructions*** (111). See MPEP § 806.05(d). Claim 17 recites executing a processor instruction, but it does not necessarily mean that the processor instruction must not come from other part of a system. Therefore, the restriction is proper.

7. As to d), claim 23 specifically recites a second field to indicate how to modify the portion of segment. Therefore, it is classified under 717/143, analysis of code format , parsing and syntax analysis.

The requirement is still deemed proper and is therefore made FINAL.

8. Claims 1-5 are rejected under 35 U.S.C. 102(e) as being anticipated by Nunomura (6,871,274).

9. As to claim 1, Nunomura taught at least :
a) fetching a first machine language instruction (tran instruction) comprising an instruction segment [TRANS 1100 0010 0001 0010] (see the dispatched instruction from the prefetch unit in col.5, lines 50-54);

10. b) responsive, or recognizing, or based on, to a trigger pattern [index] in said first machine language instruction (see machine language in fig.4), modifying said instruction segment to form a second machine language instruction (see 1001 1111 1100 0000 0000 0010 0001 0010 in fig.4, col.6, lines 27-50);

11. c) executing said second machine language instruction (see execution unit 230 connected to output of conversion unit 330 via the instruction decode unit 240 in fig.1).

12. As to the amended "fetching from memory", see the dispatched instruction from the prefetch unit in col.5, lines 50-54. As to the "executing on said processor", examiner hold that an execution of instruction had to be on processor.

13. Nunomura also taught memory for storing the instruction (see fig.122, col.5, lines 41-45).

14. As to claim 2, Nunomura modifying substituted a bit pattern of a subset of said instruction segment (see the corresponding index).

15. As to claim 3, Nunomura also repeated the fetching (see the determination of program end or not to the prefetch step in B in fig.3A).

16. As to claims 4, Nunomura was also directed to a microcode (see fig.4).

17. As to claims 5, Nunomura also included a particular execution unit (see fig.1 [230]).

18. Claims 6,7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nunomura (6,871,274) in view of Rim (6,202,143).

19. As to claims 6,7, Nunomura did not specifically show the VLIW as claimed. However, Rim taught a VLIW conversion system (see col.8, lines 8-27). It would have been obvious to one of ordinary skill in the art to use Rim in Nunomura for including the VLIW as clamed because the use of Rim could provide Nunomura the ability to accept different type of instruction formats , thereby increasing the adaptability Nunomura , and it could be achieved by predefining VLIW control parameters of Rim (e.g. the instruction length and type) into the configuration file of Nunomura so that the specific instruction type with corresponding width of the Rim's VLIW could be recognized by Nunomura , and because Nunomura also taught a variable length instruction pattern could be used (see col.12, lines 26-46), which was an indication of the applicability of a large number of instruction words or a long instruction word (see col.12, lines 46-52), such as the VLIW, in doing so , provided a motivation.

20. As to the applicant's remarks that :

a) Nunomura's compressed instruction code is unrecognizable as an instruction code in col.7, lines 30-37;

b) compressed instruction code is accessed by an instruction code conversion apparatus and not by an instruction decode unit;

c) 4 is not equal to 24;

d) increased complexity is not an advantage;

e) no desirability of modifying Nunomura to accept VLIW instructions;

f) no suggestion in the art to motivate the use of VLIW.

21. As to a) above, "unrecognizable" does not necessarily mean "is not." For example, the fact that applicant is not recognizable as an applicant does not mean that applicant is not applicant. In col.7, lines 30-37, Nunomura was able to detect unrecognizable instruction , TRAN instruction. Although the instruction was unrecognizable, it was an instruction.

22. As to b), no specific type or structure of instruction decoder has been reflected into the claim. Therefore, instruction decoder is read as any instruction decoder in general, such as instruction code conversion unit.

23. As to c) above, 4 is a segment itself.

24. As to d) , applicant failed to explain why Rim is more complex ?

25. As to e), no specific details of VLIW instruction have been reflected into the claim. Therefore, one of ordinary skill in the art should be able to recognize generally applicable VLIW into Nunomura for achieving the adaptability.

26. As to f), see response to e) above.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

27. Claim 1-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Trembly et al. (5,925,123).

28. As to claim 1, 4, Trembly taught at least :
a) fetching from memory [local memory] a first machine language instruction [virtual machine instruction] comprising an instruction segment (see fig.7 for opcode for instruction segment, col.27, lines 40-54 opcode);
b) responsive to a trigger pattern [mode] in the first machine language instruction, modifying the instruction segment to form a second machine language instruction [microcode]; and
executing on said processor said second machine language instruction (see execution of microcode in col.3, lines 20-36, see col.26, lines 16-65 for details of translation, see also translation and execution of the translated native instructions in col.25, lines 42-65. As for the memory, see instructions received from memory in col.25, line 34, col.26, line 30-34, see also col.27, lines 10-53 for the activation of execution).

29. As to claim 2, see set mode bit changed for RISC opcodes in col.27, lines 40-54 opcode.

30. As to claim 3, Trembly had repeated the fetch, and modified without intervening instruction (see the translation not requiring software interpreter in col.26, lines 10-15. For repeating fetch, see receiving the instruction form local memory in

col.16, lines 30-34, see also assembly and reassemble capabilities in col.25, lines 20-34 for background).

31. As to claim 5, see translation of the RISC, CISC and VLIW processors in col.3, lines 37-40, col.26, lines 51-68.

32. As to claims 6,7, see translation of the VLIW processor in col.3, lines 37-40, col.26, lines 51-68.

33. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Luick (6,230,260) is cited for the teaching of the VLIW identifying the branch (see fig.10, col.19, lines 57-67);

b) Bereboum (6,658,551) is cited for the teaching of the VLIW instruction fields to identify the portion of the instruction to be modified (see figs.13,14).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

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21 Century Strategic Plan

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